MAEDA et al.
Serial No. 10/714,935
Response to Office Action dated July 7, 2006

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A shift register block comprising:

at least one system of a shift register comprising ~~constituted of~~ a plurality of unit circuits in a form of cascade connection and outputting an input signal in response to a clock signal, the shift register sequentially outputting a selection signal from output-stages comprised ~~constituted~~ of the unit circuits,

wherein:

the plurality of unit circuits are disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit which is different from the unit circuits and not involved in operation of the shift register so that an output of the circuit is not supplied to the unit circuits.

Claim 2 (Original): The shift register block as set forth in claim 1, wherein:

the unit circuits are flip-flop circuits.

Claim 3 (Currently Amended): The shift register block as set forth in claim 1, wherein:

the circuit different from the unit circuits is a processing circuit which uses output of one of the unit circuits ~~constituting the shift register~~.

Claim 4 (Currently Amended): The shift register block as set forth in claim 1, wherein:

the circuit different from the unit circuits is a unit circuit for ~~constituting~~ a shift register of a different system.

Claim 5 (Currently Amended): The shift register block as set forth in claim 1, wherein:

the circuit different from the unit circuits is a processing circuit which uses output of one of the unit circuits ~~constituting the shift register~~, a unit circuit for ~~constituting~~ a shift register of a different system, or a processing circuit which uses output of the unit circuit for ~~constituting~~ the shift register of the different system.

Claim 6 (Currently Amended): The shift register block as set forth in claim 4, wherein:

the shift register block includes signal paths for the shift registers of the respective systems, the signal path being provided separately for each of the shift registers of the respective systems on both sides of a circuit alignment ~~constituted~~ of the unit circuits of the shift registers of the respective systems.

Claim 7 (Currently Amended): The shift register block as set forth in claim 5, wherein:

the shift register block includes signal paths for the shift registers of the respective systems, the signal path being provided separately for each of the shift registers of the respective systems on both sides of a circuit alignment ~~constituted~~ of the unit circuits of the shift registers of the respective systems.

Claim 8 (Currently Amended): A signal line driving circuit, comprising:

a shift register block for sequentially outputting a selection signal, so as to drive a plurality of signal lines,

wherein:

the shift register block comprises:

at least one system of a shift register comprising ~~constituted of~~ a plurality of unit circuits in a form of cascade connection and outputting an input signal in response to a clock signal, the shift register sequentially outputting a selection signal from output-stages comprised ~~constituted~~ of the unit circuits, the plurality of unit circuits being disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit which is different from the unit circuits and not involved in operation of the shift register so that an output of the circuit is not supplied to the unit circuits.

Claim 9 (Currently Amended): A data signal line driving circuit comprising:

a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal

sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block comprises:

at least one system of a shift register comprising ~~constituted of~~ a plurality of unit circuits in a form of cascade connection and outputting an input signal in response to a clock signal, the shift register sequentially outputting a selection signal from output-stages comprised ~~constituted~~ of the unit circuits, the plurality of unit circuits being disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit which is different from the unit circuits and not involved in operation of the shift register so that an output of the circuit is not supplied to the unit circuits.

Claim 10 (Original): The data signal line driving circuit as set forth in claim 9, wherein:

the sampling section carries out sampling of image data of divided image signals which are generated by dividing the image signal according to an alignment order of the data signal lines, the sampling section simultaneously carrying out sampling of the image data of the divided image signals.

Claim 11 (Currently Amended): The data signal line driving circuit as set forth in claim 9, wherein:

the image signal is an analog signal, and the circuit different from the unit circuits comprises ~~is made up of~~ at least one of a waveform shaping

circuit, a buffer circuit, a sampling circuit, and a level shifter circuit, which use outputs of the unit circuits ~~constituting the shift register~~.

Claim 12 (Currently Amended): The data signal line driving circuit as set forth in claim 9, wherein:

the image signal is a digital signal, and the circuit different from the unit circuits comprises ~~is made up of~~ at least one of a data latch circuit, a digital/analog conversion circuit, an output circuit, a level shifter circuit, and a decoder circuit, which use outputs of the unit circuits ~~constituting the shift register~~.

Claim 13 (Currently Amended): A display device, comprising:

a plurality of data signal lines;

a plurality of scanning signal lines intersecting with the data signal lines;

pixels provided for each pair of the data signal lines and the scanning signal lines;

a scanning signal line driving circuit for driving the scanning signal lines; and

a data signal line driving circuit comprising a sampling section for driving a plurality of data signal lines by sampling image data from an image signal according to a selection signal sequentially outputted from a shift register block so as to transfer the image data to the data signal lines,

wherein:

the shift register block of the data signal line driving circuit comprises:

at least one system of a shift register comprising ~~constituted of~~ a plurality of unit circuits in a form of cascade connection and outputting an

input signal in response to a clock signal, the shift register sequentially outputting a selection signal from output-stages comprised ~~constituted~~ of the unit circuits, the plurality of unit circuits being disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit which is different from the unit circuits and not involved in operation of the shift register so that an output of the circuit is not supplied to the unit circuits.

Claim 14 (Original): The display device as set forth in claim 13, wherein:

the data signal line driving circuit and the scanning signal line driving circuit are formed on a substrate on which the pixels are formed.

Claim 15 (Original): The display device as set forth in claim 14, wherein:

the pixels, the data signal line driving circuit, and the scanning signal line driving circuit include active elements, respectively, each of which is made of a polysilicon thin film transistor.

Claim 16 (Original): The display device as set forth in claim 15, wherein:

the active elements are formed on a glass substrate at a process temperature of not more than 600°C.

Claim 17 (New): A shift register block comprising:

a shift register comprising a plurality of cascade-connected unit circuits for sequentially propagating an input signal therethrough in response to a

clock signal, the unit circuits being linearly disposed so that physical spaces are provided between each adjacent pair of unit circuits; and

circuits different from the unit circuits disposed in the physical spaces between adjacent unit circuits,

wherein outputs from the respective different circuits are not supplied to any of the unit circuits.

Claim 18 (New): The shift register block according to claim 17, wherein the circuits different from the unit circuits comprise waveform processing circuits.

Claim 19 (New): The shift register block according to claim 17, wherein the circuits different from the unit circuits comprise unit circuits for a different shift register.

Claim 20 (New): A display device comprising the shift register block according to claim 17.